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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,298	12/19/2001	David N. Goldberg	10019867-1	2928

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EXAMINER	
HO, CHUONG T	
ART UNIT	PAPER NUMBER
2616	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/028,298	GOLDBERG ET AL.	
	Examiner	Art Unit	
	CHUONG T. HO	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,11-17 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-9,11-17,19-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The amendment filed 11/16/06 have been entered and made of record.

2. Applicant's arguments with respect to claims 1,3-8, 9,11-16, 17, 19-24 have been considered but are moot in view of the new ground(s) of rejection.

3. Claims 1, 3-8, 9, 11-16, 17, 19-24 are pending.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 9, 17 are rejected under 35 U.S.C. 103(a) as being obvious over Bartfai et al. (U.S.Patent No. 2003/0101367 A1) in view of Owen et al. (U.S.Patent No. 6,760,838 B2).

In the claim 1, Bartfai discloses a method of error protection comprising: detecting an error during communication between nodes in a network, said nodes separated by a link; blocking (see page 3, [0028], page 5, [0046], claim 1) further communication between said nodes in response to said detected error; unblocking (see page 3, [0029], page 6, [0046], claim 1) said blocked communication between said nodes, provided said communicating nodes have resolved said detected error, wherein said communication between said nodes is re-enabled; setting a link usage indicator in a first storage (register) by reach of said communicating nodes prior to communication there between (resetting by the adapter, see col. 2, lines 5-10, the nature of the error is indicated by specific bit position in error registers within the affected adapter) (see col.

3, lines 5-10, problem clearance is indicated when restarted completes successfully as indicated by the contents of interrupt vector registers.....Once the relevant interrupt vector register bits are reset or are no longer indicate an active error severity status).

However, Bartfai is silent to disclosing wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element.

Owen et al. disclose setting (see figure 7, col. 12, lines 55-67, bit 3, CRC Error, checking a status register, Bit 0 = 1: link OK; Bit 0 = 0: link Not OK) a link usage indicator in a first storage element by reach of communicating nodes prior to communication therebetween, and wherein each of said communicating nodes (figure 7,col. 20, lines 18-20, node ID in the register) has a corresponding position in said first storage element, and wherein said link usage indicator set (figure 6, figure 7, figure 11A) by each of said nodes is relative to said corresponding position in said first storage element (see col. 12, lines 30-35 the command register of the capability block 90 for the interface , col. 12, lines 40-45, the bits in the command register are writable by software, with the execution of the unit count field and the master host unit which automatically set).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Bartfai with the teaching of Owen to provide wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is

relative to said corresponding position in said first storage element in order to allow multiple compute elements (nodes) to read and independently clear error register logs, discard invalid data and which ensures that the user receives information received in error log registers.

6. In the claim 9, Bartfai discloses a method of error protection comprising: detecting an error during communication between nodes in a network, said nodes separated by a link; blocking (see page 3, [0028], page 5, [0046], claim 1) further communication between said nodes in response to said detected error; unblocking (see page 3, [0029], page 6, [0046], claim 1) said blocked communication between said nodes, provided said communicating nodes have resolved said detected error, wherein said communication between said nodes is re-enabled; setting a link usage indicator in a first storage (register) by reach of said communicating nodes prior to communication there between (resetting by the adapter, see col. 2, lines 5-10, the nature of the error is indicated by specific bit position in error registers within the affected adapter) (see col. 3, lines 5-10, problem clearance is indicated when restarted completes successfully as indicated by the contents of interrupt vector registers.....Once the relevant interrupt vector register bits are reset or are no longer indicate an active error severity status).

However, Bartfai is silent to disclosing wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element.

Owen et al. disclose setting (see figure 7, col. 12, lines 55-67, bit 3, CRC Error, checking a status register, Bit 0 = 1: link OK; Bit 0 = 0: link Not OK) a link usage indicator in a first storage element by reach of communicating nodes prior to communication therebetween, and wherein each of said communicating nodes (figure 7,col. 20, lines 18-20, node ID in the register) has a corresponding position in said first storage element, and wherein said link usage indicator set (figure 6, figure 7, figure 11A) by each of said nodes is relative to said corresponding position in said first storage element (see col. 12, lines 30-35 the command register of the capability block 90 for the interface , col. 12, lines 40-45, the bits in the command register are writable by software, with the execution of the unit count field and the master host unit which automatically set).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Bartfai with the teaching of Owen to provide wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element in order to allow multiple compute elements (nodes) to read and independently clear error register logs, discard invalid data and which ensures that the user receives information received in error log registers.

7. In the claim 17, Bartfai discloses a communication interconnect (figure 1); an optional display device coupled to said communication interconnect (it is inherent that an optional display device is connected to at least one node in order to monitor and

execute software programs and application (paragraphs [0002] [0003]); and a processor coupled to said communication interconnected (paragraph [0003]); blocking (see page 3, [0028], page 5, [0046], claim 1) further communication between said nodes in response to said detected error; unblocking (see page 3, [0029], page 6, [0046], claim 1) said blocked communication between said nodes, provided said communicating nodes have resolved said detected error, wherein said communication between said nodes is re-enabled; setting a link usage indicator in a first storage (register) by reach of said communicating nodes prior to communication there between (resetting by the adapter, see col. 2, lines 5-10, the nature of the error is indicated by specific bit position in error registers within the affected adapter) (see col. 3, lines 5-10, problem clearance is indicated when restarted completes successfully as indicated by the contents of interrupt vector registers.....Once the relevant interrupt vector register bits are reset or are no longer indicate an active error severity status).

However, Bartfai is silent to disclosing wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element.

Owen et al. disclose setting (see figure 7, col. 12, lines 55-67, bit 3, CRC Error, checking a status register, Bit 0 = 1: link OK; Bit 0 = 0: link Not OK) a link usage indicator in a first storage element by reach of communicating nodes prior to communication therebetween, and wherein each of said communicating nodes (figure 7,col. 20, lines 18-20, node ID in the register) has a corresponding position in said first

storage element, and wherein said link usage indicator set (figure 6, figure 7, figure 11A) by each of said nodes is relative to said corresponding position in said first storage element (see col. 12, lines 30-35 the command register of the capability block 90 for the interface , col. 12, lines 40-45, the bits in the command register are writable by software, with the execution of the unit count field and the master host unit which automatically set).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Bartfai with the teaching of Owen to provide wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element in order to allow multiple compute elements (nodes) to read and independently clear error register logs, discard invalid data and which ensures that the user receives information received in error log registers.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3-8, 11-16, 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over combined system (Bartfai – Owen) in view of Lindsay (U.S.Patent No. 6,654,908 B1).

In the claim 3, Bartfai et al. disclose the limitations of claim 1 above.

However, the combined system (Bartfai – Owen) are silent to disclosing wherein said detection of said error causes a generation of an error indicator, said error indicator stored in a second storage element.

Lindsay discloses wherein said detection of said error causes a generation of an error indicator, said error indicator stored in a second storage element (figure 2, col. 6, lines 27-30, if the status register is set to indicate an error, the compute element reads the tag register for the specific error type).

Both Bartfai, Owen, and Lindsay disclose error detection. Lindsay recognizes wherein said detection of said error causes a generation of an error indicator, said error indicator stored in a second storage element. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined system (Bartfai – Owen) with the teaching of Lindsay to detect of said error causes a generation of an error indicator, said error indicator stored in a second storage element in order to allow multiple compute elements (nodes) to read and independently clear error register logs, discard invalid data and which ensures that the user receives information received in error log registers.

10. In the claim 4, Bartfai discloses the limitations of claim 1 above.

However, the combined system (Bartfai – Owen) is silent to disclosing activating a blocking agent to provide said blocking of said communication, said blocking agent activated in response to said generation of said error indicator.

Lindsay discloses activating a blocking agent to provide said blocking of said communication, said blocking agent activated in response to said generation of said error indicator (see figure 2, col. 6, lines 27-30).

Both Bartfai, Owen, and Lindsay disclose error detection. Lindsay recognizes activating a blocking agent to provide said blocking of said communication, said blocking agent activated in response to said generation of said error indicator. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined system (Bartfai – Owen) with the teaching of Lindsay to activate a blocking agent to provide said blocking of said communication, said blocking agent activated in response to said generation of said error indicator in order to allow multiple compute elements (nodes) to read and independently clear error register logs, discard invalid data and which ensures that the user receives information received in error log registers.

11. In the claim 5, Bartfai discloses resolving of said detected error is performed by each of said communicating nodes, and is in a manner appropriate for each node (see paragraph 29 , 30).

12. In the claim 6, Bartfai discloses the limitations of claim 1 above.

However, the combined system (Bartfai – Owen) are silent to disclosing generating multiple clearing by said nodes, wherein each of said nodes generating one of said multiple clearing indicators subsequent to it said resolving of said error, wherein each of said clearing indicators corresponds to an associated corresponding position

relative to said nodes, and wherein each of said clearing indicators resets a link usage indicators set by each of said nodes.

Lindsay discloses generating multiple clearing indicators (see col. 4, lines 20-22) by said nodes, wherein each of said nodes generating one of said multiple clearing indicators subsequent to it said resolving of said error, wherein each of said clearing indicators corresponds to an associated corresponding position relative to said nodes, and wherein each of said clearing indicators resets (see col. 3, lines 65-67) a link usage indicators set by each of said nodes.

Both Bartfai, Owen, and Lindsay disclose error detection. Lindsay recognizes generating multiple clearing by said nodes, wherein each of said nodes generating one of said multiple clearing indicators subsequent to it said resolving of said error, wherein each of said clearing indicators corresponds to an associated corresponding position relative to said nodes, and wherein each of said clearing indicators resets a link usage indicators set by each of said nodes . Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined system (Bartfai – Owen) with the teaching of Lindsay to generate multiple clearing by said nodes, wherein each of said nodes generating one of said multiple clearing indicators subsequent to it said resolving of said error, wherein each of said clearing indicators corresponds to an associated corresponding position relative to said nodes, and wherein each of said clearing indicators resets a link usage indicators set by each of said nodes in order to allow multiple compute elements (nodes) to read and

independently clear error register logs, discard invalid data and which ensures that the user receives information received in error log registers.

13. In the claim 7, Bartfai discloses a first storage element and second storage element are disposed in said link (figure 2, reference 162, paragraph [0003]. Memory in adapter is interpreted as storage element and is disposed in a link connected to the adapter.

14. In the claim 8, Bartfai discloses a first storage element and second storage element are disposed in each said node (paragraph [0004]); memory in a node is interpreted as storage element disposed in each node.

15. In the claim 11, claim 11 is rejected the same reason of claim 3 above.

16. In the claim 12, claim 12 is rejected the same reason of claim 4 above.

17. In the claim 13, claim 13 is rejected the same reason of claim 5 above.

18. In the claim 14, claim 14 is rejected the same reason of claim 6 above.

19. In the claim 15, claim 15 is rejected the same reason of claim 7 above.

20. In the claim 16, claim 16 is rejected the same reason of claim 8 above.

21. In the claim 19, claim 19 is rejected the same reason of claim 3 above.

22. In the claim 20, claim 20 is rejected the same reason of claim 4 above.

23. In the claim 21, claim 21 is rejected the same reason of claim 5 above.

24. In the claim 22, claim 22 is rejected the same reason of claim 6 above.

25. In the claim 23, claim 23 is rejected the same reason of claim 7 above.

26. In the claim 24, claim 24 is rejected the same reason of claim 8 above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG T. HO whose telephone number is (571) 272-3133. The examiner can normally be reached on 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

01/31/07

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